# A Low Power GaAs MESFET Monolithic Downconverter for Digital Handheld Telephone Applications

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Abstract:

A monolithic GaAs MESFET downconverter for 1.9 GHz digital handheld telephone applications has been designed and fabricated. The downconverter operates from a single supply, and uses no dual gate or series biased FETs, which allows operation at lower supply voltages. The circuit exhibits 22 dB of conversion gain and 3.9 dB noise figure at a bias of 2.7 V and 5 mA, with a LO drive of -10 dBm. For a supply voltage of 1.25 V and a LO drive level of -13 dBm, conversion gain of 17.2 dB and noise figure of 4.3 dB is obtained.

## Introduction

Portable digital telephones operating in the 1.9 GHz range require low cost front ends which operate at low voltages and currents while still exhibiting high conversion gain and low noise figure. In a handheld phone, minimizing weight and increasing talk time are primary driving factors in the design. Lowering supply voltage decreases the numbers of batteries required, thereby reducing the weight of the handset, while lowering current consumption increases talk time. For low voltage, low current applications at frequencies of 1 GHz and above, GaAs MESFET technology becomes very attractive [1-4].

In this paper, we report a low noise GaAs MESFET downconverter for use in the 1.9 GHz range. The circuit has been designed to minimize performance variation with process and temperature, and is fabricated using a process designed for manufacturability. The downconverter shows good performance at supply voltages below 1.8 V and an LO power of -15 dBm. The downconverter is provided with an enable input which allows it to be shut off when not in use, thereby limiting current consumption in the handset.

## Design

A block diagram of the downconverter is shown in Figure 1. The chip is fabricated using the E/D MESFET process available in Motorola's CS-1 fab. This is a uniplanar, self-aligned process featuring refractory gates and ion-implanted active regions [5]. The active devices are D-mode MESFETs in a self-biased configuration as shown in Figure 2. This bias arrangement was chosen because of its stability with respect to process, temperature, and supply variation and also because of its simplicity. The use of single gate FETs allows operation at lower voltages than dual gate MESFETs, which are typically operated in cascode. The enable function is provided by using an E-mode MESFET in bias line to the active devices.

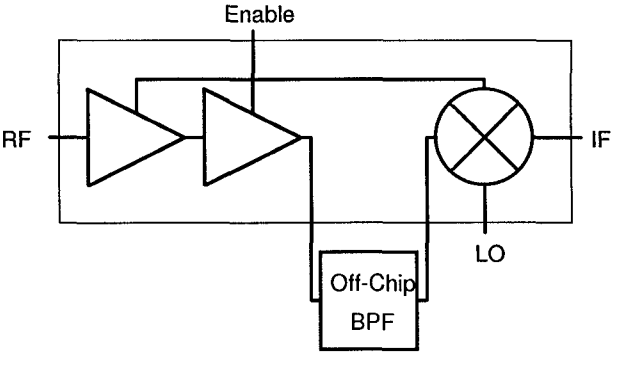


Figure 1. Block diagram of the downconverter.

A schematic of the gain stage is shown in Figure 2. The high-pass matching topology was chosen for several

reasons. First, it is the most compact approach available. Second, it minimizes the number of spiral inductors, which are relatively lossy elements. Third, it provides attenuation of the image frequencies in the low side LO mixer, which eases the requirements of the external image filter. For a 1.9 GHz RF signal and a 110 MHz IF, the image is attenuated by more than 10 dB due to the low end gain rolloff of the amplifier. This attenuation increases as the IF frequency is increased. Finally, the high pass matching network allows easy application of the bias.

All of the 1.9 GHz matching is performed on the chip. This approach reduces the parts count and complexity of the handset, although it accounts for an increase in the downconverter noise figure due to the lower Q of the on-chip matching elements. The entire downconverter occupies a die area of 60 x 90 mils.

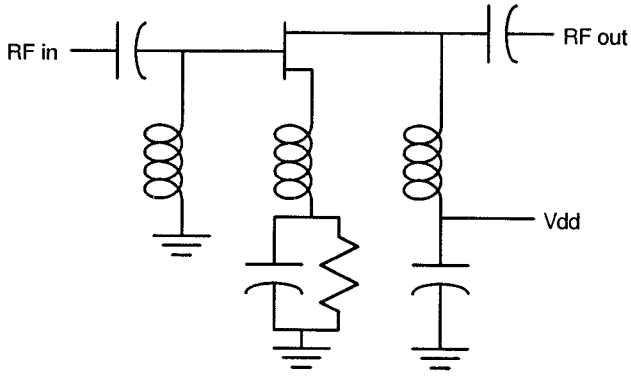


Figure 2. Schematic of a single gain stage.

The mixer is of the single gate FET transconductance type [6], with the LO and RF signals applied to the gate, shown in Figure 3. The LO and RF signals are combined at the gate of the FET using a lumped element Wilkinson power combiner. The output of the FET is matched to 50 ohms using an off-chip low pass matching network. For narrow IF bandwidths, a single inductor can be used. Using two chip inductors and a capacitor, a 40 MHz IF bandwidth centered at 100 MHz was obtained.

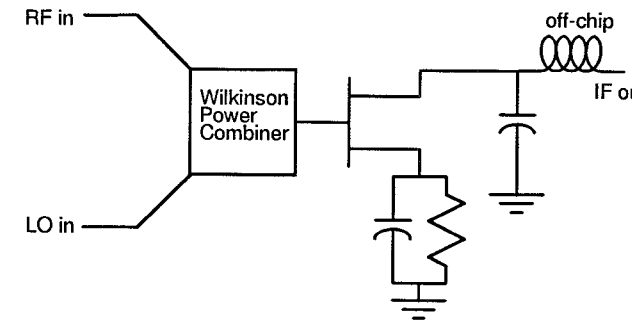


Figure 3. Schematic of the mixer.

Measured performance

Conversion gain and noise figure of the downconverter are shown in Figure 4 as a function of supply voltage. Although the chip was designed for a three cell supply, (Vdd = 2.7 V min), it shows good performance below 1.8 V, indicating that it can be used in a two-cell system. Figures 5 and 6 show downmixer performance as a function of supply current and LO drive power. The losses associated with the image filter, (about 1 dB), and the test fixture, (about 0.25 dB per port), are included in the data given here.

When operated at 2.7 V and 5 mA, with an LO drive level of -7 dBm, the third order intercept point is 3 dBm at the output. LO-IF, RF-IF, and LO-RF isolation were all better than 30 dB for the downconverter.

It is worthwhile to compare the results presented here to similar circuitry reported elsewhere. The downconverter reported in [2] exhibits lower conversion gain at significantly higher dc power consumption and LO drive levels. The results given in [4] using dual-gate FETs shows comparable gain and current consumption at higher supply voltages and frequencies an octave lower than those reported here. In this last reference, off-chip RF matching is also required.

Conclusions

A monolithic GaAs MESFET downconverter for 1.9 GHz portable telephone applications has been demonstrated using a MMIC process suited to high-volume production. The circuit shows good gain and noise performance at low supply power and LO drive levels, which implies reduced weight and increased talk time for the handset.

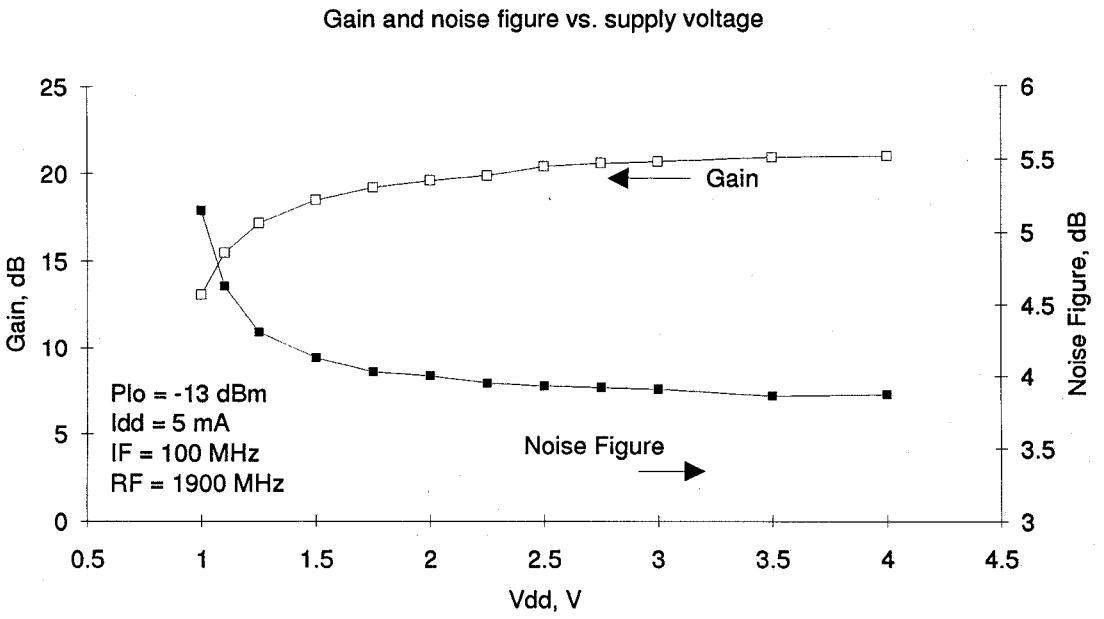


Figure 4. Downconverter performance vs. supply voltage.

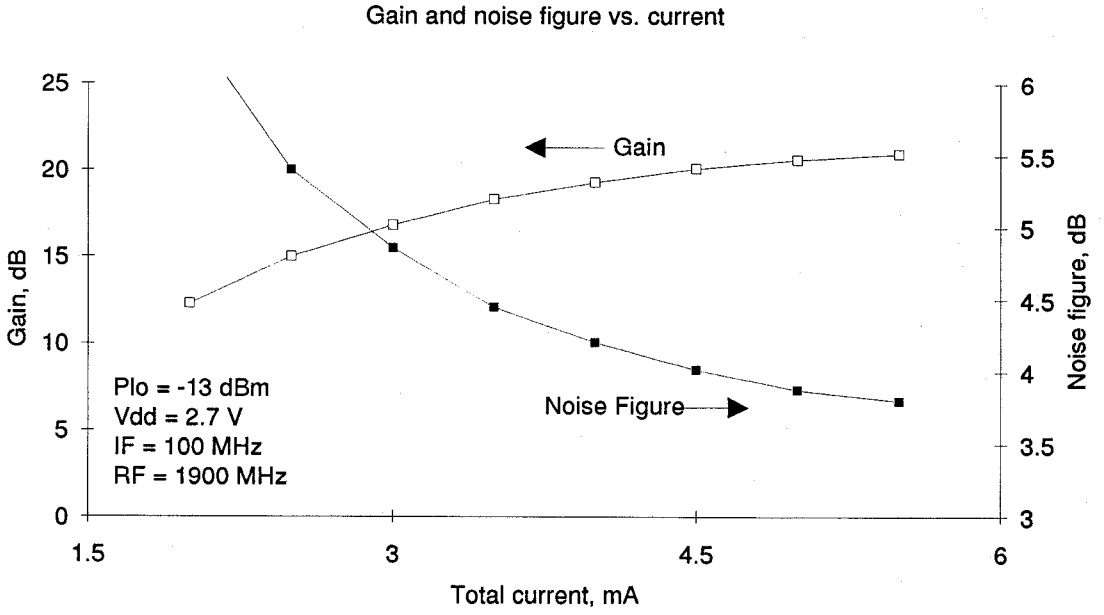


Figure 5. Downconverter performance vs. supply current.

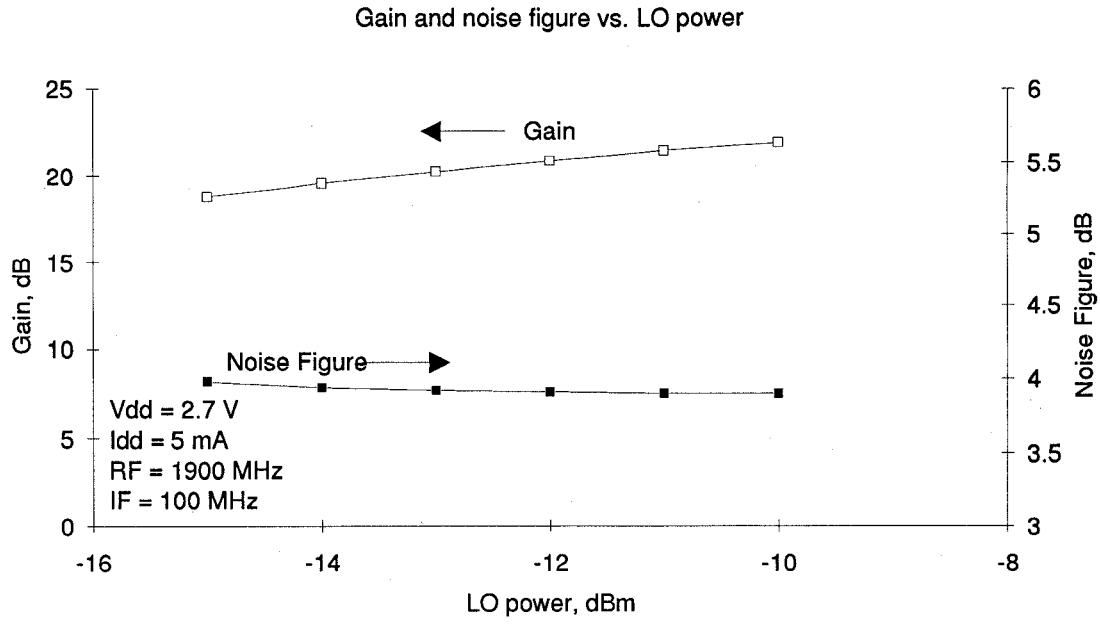


Figure 6. Downconverter performance vs. LO drive.

Acknowledgments

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References:

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